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THE NECESSITY FOR A DoD CAPABILITY IN SUPERCONDUCTING ELECTRONICS

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The technologies of superconductor electronics and hybrid superconductor-semiconductor electronics offer a unique potential for more compact systems that would afford higher performance and lower power consumption than does the present semiconductor electronics. This paper discusses current efforts in superconductor electronics and warns of probable future Department of Defense (DoD) dependence on foreign capabilities in this critical technology. The paper describes selected systems on DoD "needs" lists and recommends the establishment of programs and processing capabilities that will assure the realization of the many essential benefits offered by superconducting electronics.

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FOREWORD

We are working at a time when an aura of great expectations accompanies the research and development work being carried out on the new high-transition-temperature superconducting oxides. At such a time, the advocacy of a vigorous effort in Nb-based and NbN-based low-temperature superconducting electronics requires justification. This justification is twofold.

First, Nb and NbN processing technologies have attained sufficient maturity that films of very high quality are routinely produced. Moreover, large arrays of Josephson junctions can be made with uniform and reproducible characteristics and can be thermally cycled repeatedly without degradation. These facts indicate that innovations in devices, circuits, and systems and their architectures can proceed apace, and that highly useful devices and systems can be produced and utilized in the near term. On the other hand, difficult obstacles are inherent in the processing of high-temperature superconductors. When these are overcome, all of the accomplishments achieved with low-temperature superconductors may be reproduced with high-temperature materials. A strong capability in low-temperature superconducting technology may not be a sufficient precursor for assuring the attainment of a strong competitive position in high-temperature superconducting electronics, but it is most likely a necessary one.

Second, by virtue of the differences in their energy gaps, low- and high-temperature superconductors will fill unique but different needs. For example, since intrinsic switching times are generally inversely proportional to the energy gap, it will be possible to make faster switches with materials of high critical temperature (T_C). Assuming that the same kind of logic is used for both high-T_C and low-T_C circuits (e.g., conventional latching logic), the high-T_C circuits should have a much higher voltage and, because of the greater noise, a much higher current. (If nonlatching logic were used, the power could be lower.) Switching energies should thus approach those of semiconductors. Accordingly, there would be the associated limitations arising from power availability and from heat removal. The latter factor places limitations on device density and introduces transit delays that may restrict the ultimate speed of the overall system. For applications where only modest numbers of the fastest switching elements are

required, high-T_C electronics technology may be desirable. On the other hand, although low-T_C switching elements may be somewhat slower than high-T_C elements, they are significantly faster than their semiconducting counterparts, and their switching powers are about a factor of 1,000 less. Consequently, in applications where high-density logic circuits are required for their smaller critical-path transit delays, low T_C technology is very attractive. Finally, the magnitude of the flux quantum impacts on the density of the superconducting memory, be it of high T_C or low T_C. The ratio of the flux quantum (2.07×10^{-15} Wb) to the critical current determines the self-inductance of the smallest ring of radius R that can be part of the superconducting memory. That inductance is roughly proportional to RlogR, and thus it determines the size of the ring and therefore the density of any mass memory that is structured in superconducting technology. This memory is most probably less dense than its semiconducting counterpart.

Taking all the above factors into account, one can imagine a hybrid such as a surveillance system in which high-T_C technology is used for the sensor and processor, low-T_C technology is used for ultrafast analog-to-digital converters and fast-cache memory, and semiconductor technology is used for moderate-access mass memory. Although this report does not dwell on it, such a hybrid system may indeed be the wave of the future.

Ted G. Berlincourt

PREFACE

In January 1988, the Institute for Defense Analyses (IDA) undertook Task T-D2-566 in superconductivity studies at the request of Dr. Ted G. Berlincourt, Director of Research and Laboratory Management, Office of the Deputy Director of Defense Research and Engineering (Research and Advanced Technology). To initiate the studies, IDA held a workshop on January 28-29, 1988. The participants were superconductivity experts who represented the three armed services and other Government activities. A major goal of the workshop was to encourage coordination of effort among the services and the sharing of knowledge, experience, and future plans. The proceedings of the workshop and the recommendations of the participants to the Office of the Secretary of Defense are included in IDA Memorandum Report M-482.

Among the recommendations was the establishment of a niobium "foundry" to fabricate the superconducting electronic devices of high value to the services. A DoD-IDA committee was formed to consider the best way to approach the deeper study and possible implementation of that recommendation. The committee convened a workshop on September 26-27, 1988, with participation augmented by members of academia, industry, and non-DoD Government agencies. The larger group examined the need for a DoD facility and the nature of the potential user community if the facility were made available to the general United States technical community. The establishment of the facility, now referred to as the Superconducting Electronics Fabrication Facility (SEFF), was laid out to occur over a 5-year period together with a parallel program of increasingly sophisticated demonstration vehicles. A cost schedule was also laid out. The deliberations of the group and its full recommendations are reported in IDA Document D-560, *A Superconducting Electronics Fabrication Facility (SEFF) for DoD* (Ref. 1). Most important for the purposes of this paper is the recommendation of Ref. 1 that DoD undertake to establish both SEFF and the parallel program.

This paper goes the next step. It examines some representative scenarios and applications specific to the needs of various segments of DoD. It compares how current technology and superconductive electronics might handle the computational loads demanded by the various applications. Moreover, it includes recommendations on

programs that, in conjunction with SEFF, would comprise a balanced, aggressive total approach to the development of superconducting electronic systems that would be of great value both to the U.S. military and to U.S. commercial competitiveness.

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During the course of this study, many people, both in and outside of IDA, provided guidance and viewpoints that were of great value in writing this report. Drs. M.N. Nisenoff, F. Bedard, and N. Welker participated in discussions with DoD and armed service staff and provided input. Drs. B. Paiewonsky, G.J. Iafrate, R.M. Christiansen, K. Kramer, J. Hiller, and J.P. Boris and their staffs provided discussions and information on armed service applications of electronic devices. Dr. R.H. Van Atta shared his perspective of DoD's relationship to the semiconductor industry. Special thanks are due to Drs. Bedard and Nisenoff for the circuit analyses carried out in Chapter III, "Demonstration Vehicles," and to Messrs. R.L. Goodwin, R.M. Christiansen, and J. Grantham for the values of the computational load requirements used in Sections III-A and III-B.

ABSTRACT

The technologies of superconductor electronics and hybrid superconductor-semiconductor electronics offer a unique potential for more compact systems that would afford higher performance and lower power consumption than does the present semiconductor electronics. This paper discusses current efforts in superconductor electronics and warns of probable future Department of Defense (DoD) dependence on foreign capabilities in this critical technology. The paper describes selected systems on DoD "needs" lists and recommends the establishment of programs and processing capabilities that will assure the realization of the many essential benefits offered by superconducting electronics.

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EXECUTIVE SUMMARY

A. INTRODUCTION

In June 1989, IDA Document D-560 (Ref. 1) explored Department of Defense (DoD) needs for high-speed, low-power-dissipation electronic systems and, as a consequence, recommended a vigorous effort in structuring a DoD-oriented capability in superconducting electronics. Extending that work, an IDA group met with representatives of DoD agencies and laboratories and listened to briefings describing specific program needs and scenarios and the computational loads that they impose on the engineering systems involved. A comparative study was then made of the characteristics that those systems would have in both semiconductor and superconductor electronics technology.

B. BACKGROUND: ELECTRONICS TECHNOLOGY IMPACT ON DoD

In the era following World War II, electronics advances in both the defense and the space efforts made a big impact on the U.S. lifestyle and on U.S. commercial competitiveness. A decade ago, most of the world's semiconductor electronic chips were made in the United States. Today, about half are made here and the rest are made abroad, chiefly in Japan. Foreign-made chips now supply the major part of the needs of U.S. computational and other sophisticated electronic systems. DoD felt stressed by its dependency on foreign sources. In an effort to alleviate that stress, the U.S. semiconductor manufacturing institute, SEMATECH, was formed.

A comparable relationship between the United States and Japan is forming with respect to the emerging industry of superconducting electronics. Japan has at least four facilities dedicated to the making of complex superconductive niobium circuitry. Of these, Fujitsu, Hitachi, and the Electrotechnical Laboratory (ETL) have all built 4-bit niobium microprocessors operating at a clock rate above 1 GHz. In building its device, ETL made seven major advances, as well as demonstrating the feasibility of producing a working prototype of a Josephson computer. The United States does not have a single facility dedicated to the making of such complex superconducting circuitry.

C. DEMONSTRATION VEHICLES

As a result of its conversations with representatives of DoD laboratories and agencies, the IDA group selected three prototype systems or "demonstration vehicles" (DVs) on which to base a comparison of the capabilities of semiconductor and superconductor electronics technologies to handle heavy computational loads on a variety of platforms. The first DV involves an airplane (on a vital mission) using electronic warfare jamming in response to potential threats. Between jamming operations, the plane's electronics must accept radar pulses with a peak density exceeding 10^6 pulses/sec, perform surveillance, identify emitters, and establish and maintain tracks. The second DV involves an infrared focal plane array with signal processing. The scenario is typical of Strategic Defense Initiative (SDI) studies in midcourse discrimination and describes waves of 5,000 reentry vehicles and 350,000 decoys. The third DV involves an important component of a very highly advanced computing system, the crossbar switch. This switch permits any one of n processors in a parallel architecture to access any one of the m memories in a shared memory bank. In all three cases, the electronic systems are considered in both semiconductor and superconductor technologies. In those cases where design parameters are considered in detail, at least an order-of-magnitude less power is required by the superconducting system even when refrigerastion is included. In the second case, selecting the superconducting electronics makes the difference between getting the system aboard a present-day satellite and not being able to do so. In case three, the demands of the system in power and speed restrict design considerations to superconducting technology.

D. SEFF

The establishment of a Superconducting Electronics Fabrication Facility (SEFF) and the implementation of a demonstration vehicle program would entail a 5-year effort and a total budget of about $50 million each. Initially a niobium line would be installed, to be followed a year or two later by a parallel niobium nitride line. A high-temperature superconductor line would follow only when the technology became mature.

E. CONCLUSIONS AND RECOMMENDATIONS

The DVs outlined in Section C permit comparisons of the performances of semiconductor and superconductor technologies in three scenarios representative of future critical electronics problems facing the DoD. In all three scenarios semiconductor power input is comparatively very high, and in two scenarios only superconductor technology is

likely to permit mission accomplishment. In the light of these results, it is concluded that superconducting electronics must be readily available to the DoD.

In the light of the competitive position of the offshore superconducting electronics fabrication facilities now in existence and the potentially crippling dependency of DoD on those facilities, it is strongly recommended that SEFF be established now, and that the parallel program of DVs be initiated.

I. INTRODUCTION

In June 1989, the authors of this paper edited IDA Document D-560 (Ref. 1), which explored future DoD needs for ultrahigh-speed, low-power superconducting electronic systems. That document recommended a vigorous effort in structuring a U.S. capability in superconducting electronics that would serve DoD contractors, academia, and the private sector. Among the benefits to the United States from such an effort would be an industrial edge in competition with a very aggressive and very innovative Japanese effort in the same field. The program would be led by the DoD and would consist of a two-pronged 5-year effort. First, the Superconducting Electronics Fabrication Facility (SEFF) would be established. Second, there would be a parallel program to target the building of a series of increasingly sophisticated demonstration systems or "vehicles" at SEFF. SEFF would publish design manuals compatible with state-of-the-art technology, and users would submit their designs through an electronic design communication system. The completion of a series of demonstrations would highlight for a concerned community the growing capabilities of SEFF and would, in fact, let it be known that both a new facility and a trained cadre of technologists had come on line.

This paper picks up where Ref. 1 left off. The SEFF study committee members met with various staff members of laboratories of the armed services and of other DoD agencies and asked them to provide specific program needs and scenarios, both present and future, wherein present semiconductor technology is severely strained in trying to meet the computational loads entailed. Several scenarios were then selected from those presented, the computational loads were sketched out, and the size and power needs of the required electronics were estimated for both semiconductor and low-temperature superconducting technologies. The feasibilities of accomplishing the missions in the two technologies were then compared. The comparisons demonstrate definitively the DoD's need to advance aggressively in the direction of establishing SEFF.

II. THE IMPACT OF ELECTRONICS TECHNOLOGY ON DoD

A. BACKGROUND

In the era since World War II, the application of electronics in all tactical and strategic systems of the armed forces has been so widespread and so essential that an awareness of it overflowed into the everyday consciousness of the average American. It was made manifest in the popular literature and the recreational dramatic media of cinema and television. Achievements in military electronics were paralleled by achievements in space electronics, beginning with Sputnik and including all the Soviet and U.S. missions. Supercomputers became the icon of advanced electronic achievement. Popular familiarity with sophisticated electronics was further promoted by the rapid transfer of the new electronic technologies to the private sector and the use of commercial electronic products in the American home. These products included audio-video systems and personal computers. Most of the former products and a large part of the latter are made overseas.

A decade ago, most of the semiconductor electronic chips used in the world were made in this country. Today only half of them are made here, and those generally find their way into industrial controls. Those found in electronics applications are, for the most part, made offshore. A dramatic example of this change is to be found in equipment of the American radio amateur or "ham." In the vacuum tube days of before and after World War II, a ham frequently made his own gear and sometimes purchased it from such memorable U.S. manufacturers as Hammarlund, National, Hallicrafters, and RCA. In the transistor era, outstanding equipment was made by such U.S. companies as Drake, Atlas, Motorola, and Heath. By the dawn of the '80s, the bulk of ham radio equipment, heavily dependent on integrated circuits, bore such brand names as Icom, Kenwood, Yaesu, KDK, and Azden, and those brands dominate the U.S. market to this day. Suffice it to say that the latter are all Japanese, and that very little American-made amateur communication equipment is to be found today.

This situation is representative of a more widespread phenomenon that seriously affects present and future DoD needs and that lies at the core of this report's message. As

the sophistication of defense technology grows, the challenge of closing the gap between the computational power demanded by DoD requirements and the computational power commercially available drives the need to exploit new and promising technologies and to diminish dependency on offshore sources to meet those needs. For example, there are now a number of DoD initiatives with pressing needs for signal and data processing in systems on land, on sea, in the air, or on space-based platforms that demand close to 10^9 instructions per second. In meeting these needs, new technologies must be compared with the semiconductor technologies that are nearing the limitations imposed by power density and by the finiteness of the speed of signal transmission, i.e., the speed of light.

B. SEMICONDUCTORS

The topic of semiconductors encompasses silicon technology mainly and gallium arsenide technology to a lesser extent. Up to perhaps a decade ago, the name Silicon Valley was synonymous with U.S. leadership in innovating the designs of new chips and in fabricating both the chips--random access memory (RAM), read-only memory (ROM), logic units, microprocessors--and the end products in which they were used, e.g., the computers themselves. The prospering of the industry made available to DoD, as well as to the Department of Energy (DOE) and the National Aeronautics and Space Administration (NASA), the resources for supplying the electronics needed for major programs of both domestic and global importance. In the intervening years of the '80s, there has been a serious erosion of the domestic semiconductor technology base. The United States has lost the lead in innovation, as well as the industrial lead in high-volume silicon devices, to offshore competitors (Ref. 2).

A recent Defense Science Board (DSB) Task Force Report (Ref. 3) pointed out that, although procurement by the DoD is relatively insignificant to the U.S. semiconductor industry, the existence of a healthy U.S. semiconductor industry is of vital importance for the national defense. For this reason, the report strongly encouraged DoD support for the establishment of a U.S. semiconductor manufacturing institute by a consortium of U.S. manufacturers. The institute, known as SEMATECH, has since been formed, and protocols for cooperation with DoD have been established. Among other ways in which DoD has attempted to meet the needs discussed here is the establishment of the Metal Oxide Semiconductor Implementation Service (MOSIS). MOSIS is sponsored by the Defense Advanced Research Projects Agency (DARPA) and is operated by the Information Sciences Institute of the University of Southern California (Ref. 1). It is a fabrication facility that

allows users to submit their designs in accord with certain design rules and to obtain their very-large-scale integrated (VLSI) devices with a turnaround time of from 1 to 4 months.

Gallium arsenide, mentioned above, has not yet become a serious competitor with silicon (Ref. 4) in most applications. To date, silicon technology has achieved levels of integration of the order of more than a million transistors per square centimeter, whereas gallium arsenide technology has achieved integration levels only of the order of 10,000. The completion of the Cray-3 supercomputer, based on gallium arsenide, will hopefully demonstrate the full potential of that technology. It is hoped to achieve clock speeds of 300 MHz, equalling speeds of the best silicon supercomputers. The further miniaturization of silicon chips is impeded by the amount of heat already generated by the high transistor density and the concomitant amount of cooling required. Specifically, the input power required by semiconductor technology and the problems of heat removal place limitations on the utilization of that technology and force the exploration of alternate approaches. That situation takes us to our next topic.

C. SUPERCONDUCTORS

During the past decade, remarkable progress has been made in exploiting the unique capabilities of superconductivity in digital electronics. Very-large-scale levels of integration on a chip have been achieved in small demonstration systems. Such VLSI circuits have operated with logic delays one-twentieth that of semiconductors while dissipating roughly one-thousandth the power. They exploit the well-developed technology of low-temperature superconductive materials and operate at liquid helium temperatures (4 K). The computational performance per unit power, even when account is taken of the unregulated power required for refrigeration, is of the order of 20 times that of the most highly developed semiconductors. The capacity of this technology to handle heavy computational loads in shorter time intervals and with smaller demands for power and weight than is required by silicon technology must not be ignored. The application of this technology to military systems of the future may be the essential step for success.

D. THE JAPANESE POSITION

Japan's $300 billion annual electronics sales significantly overshadow those of the United States. In superconducting electronics, powerful Japanese consortia are forging ahead of their U.S. counterparts. All of the recent superconducting electronics advances have been the products of a long-term (about 10-year) Japanese program to develop,

demonstrate, and evaluate very-high-speed technologies. In Japan, at least four industrial centers are dedicated to the design, fabrication, and evaluation of superconducting electronic devices. They are Electrotechnical Laboratory (ETL), Fujitsu, Hitachi, and NEC. Scientists at Fujitsu have fabricated and operated a 4-bit Josephson microprocessor at a clock rate above 1 GHz (Ref. 5). They intend to use the new technology to demonstrate a superconductor-semiconductor hybrid computer. ETL has built a fully packaged operational system consisting of four niobium-based LSI chips--one for arithmetic and logic operations, one for sequential control, one for storing instructions in ROM, and one for RAM (Ref. 6). This system, the ETL-JC1, is a 4-bit microprocessor using a 3 μ design rule and has a 6.2 mW power dissipation. It is reported that building this device required seven major technical advances and demonstrated the feasibility of producing a working prototype of a Josephson computer.

The Japanese government vigorously supports superconducting electronics technology through many initiatives, but there is not a single facility in the United States capable of fabricating, for DoD contractors, superconducting chips of the complexity routinely available in Japan. DoD contractors would have to obtain such circuits from abroad. The dangers of DoD dependency on foreign sources for critical semiconductor devices, as cited in the DSB report, are equally valid for superconductor devices. The possible exploitation of such a dependency by a foreign power is openly discussed in a recent book by Morita and Ishihara (Ref. 7). The United States is vulnerable. The establishment of a U.S. Superconducting Electronics Fabrication Facility (SEFF) to ward off this vulnerability has been discussed in an earlier report (Ref. 1).

III. DEMONSTRATION VEHICLES

Electronic technologists from DoD laboratories and agencies have suggested several prototypes or "demonstration vehicles" (DVs) to illustrate the relative performances of semiconductor and superconductor electronics in handling the heavy computational loads expected in some important future defense scenarios. From the DVs suggested, three have been selected for discussion below.

A. ELECTRONIC WARFARE (EW)

An airplane is on an important mission in support of military operations. In carrying out its mission, it must respond to potential threats to itself and does so by engaging in tactical EW jamming. It is assumed that the onboard equipment must handle surveillance over broad radiofrequency (RF) ranges, detecting both friendly and hostile emissions. It accepts radar pulses with peak densities exceeding 10^6/sec and performs real-time emitter location over a 360 deg field of view. In addition to performing these tasks, the plane must maintain emitter tracks and do these operations in a time very short compared to the total time dedicated to jamming operations. The computational loads for the problem are given by Table 1. It is assumed that in Josephson technology the electronics is characterized by a clock rate of 2 GHz, a gate delay of 9 psec, a power dissipation of <4 μW/gate, and a density of 10^4 gates per chip. In bipolar silicon, the clock rate is taken to be 330 MHz and the gate delay 200 psec. Comparative results are shown in Table 2. The superconducting electronics can handle the task with a smaller package of less than a 100 cm^3 volume and a total power dissipation of less than 2 watts. The highest performance level of silicon requires a larger volume and a power dissipation of the order of 7,500 watts. Including the additional power for refrigeration for the superconducting system, there is still an order-of-magnitude difference in the power requirements in favor of Josephson technology.

Table 1. Estimates of Present and Future EW Computational Requirements*

Requirement	Time Period	
	1985-95	Post-1995
Input Data Ensembles**		
Pulse Rate, pps	100,000-500,000	1,000,000-10,000,000
Parameter Field Width, bits	60-180	100-300
Central Processing Unit (CPU)		
Clock Frequency, MHz	1-200	50-1,000
Word Length, bits	1-64	16-64
Fast Storage (ROM, Virtual, etc.)		
Capacity, Mbytes	1-10	5-100
Access Time, nsec	50-25	25-2.5
Window-Addressable Memory (WAM)		
Depth, bits	Up to 96	128-368 @ 25 nsec; some on-chip processing
Slow Storage		
Capacity, Mbytes	10-1,000	100-1,000,000
Access Time, msec	~ 20	20-2.5

* Source: Ref. 8.

** These include radio frequency (RF), pulse repetition interval (PRI), and direction of arrival (DOA), obtained from various sensors.

Table 2. Estimates of EW Electronics in Both Silicon and Josephson Technologies*

	System Technology**	
	Silicon Bipolar†	Josephson
Processor		
Number of Logic Gates	1,130,000	124,000
Number of Chips	75	13
Power Dissipation, watts	2,500	0.5
Fast Memory (Cache)		
Number of Bytes		256,000
Number of Chips	128	128
Power Dissipation, watts	4,900	1
Read-Only Memory		
Number of Bytes		128,000
Number of Chips		32
Power Dissipation, watts		0.064
Total Size, cm^3		85
Total Chip Count		173
Total Power, watts	7,400††	1.6 @ 4 K

* Source: Ref. 9.

** Slow memory components are not included.

† Operations are implemented in the highest performance device, as in the NEC SX3 supercomputer.

†† Without cooling.

B. INFRARED FOCAL PLANE ARRAY WITH SIGNAL PROCESSING

In a typical Strategic Defense Initiative scenario, "the enemy" has launched an attack consisting of one or more waves of missiles, where each wave consists of 5000 reentry vehicles (RVs) and 350,000 decoys. The sensor platform in space must resolve closely spaced objects, track the objects, discriminate RVs from decoys, and communicate the information to a battle manager. The platform carries a highly advanced optical system that images targeted objects and clusters of objects onto a focal plane array (FPA) of infrared (IR) sensors. Initially, the outputs of the individual sensors are preprocessed to correct for detector nonuniformity and to discriminate signals due to real targets from those due to background. The FPA in this scenario has 81,920 elements, 4-color capability, and a framing time of 10 sec. Three processors are involved in the various tasks of the mission. For comparison, the electronics architecture is modeled in both silicon and niobium, representing semiconductor and superconductor technologies. For silicon, very-high-speed integrated circuit (VHSIC) chips with state-of-the-art analog and digital circuitry are assumed and power estimates are made; for niobium [i.e., low-temperature superconducting (LTS) technology], comparable studies are carried out. The comparison between the two technologies is given in Table 3. The result is that for silicon 23,400 watts of (regulated) power is required (at room temperature), and for niobium 6.1 watts (at 4.2 K). Assuming that 750 watts of unregulated cooling power is required per watt of power dissipation, LTS technology requires 4.6 kW of unregulated power and a negligible amount of regulated power, compared to 23.4 kW of regulated power required in the silicon case. To date, power sources of no more than 10 kW have been placed aboard a satellite. The differences in power and weight may well determine whether the mission can be accomplished. It appears that superconducting electronics may be necessary.

C. THE SUPERCONDUCTIVE CROSSBAR SWITCH*

Many DoD systems demand the utmost in high-performance computing technology. One system may require a special-purpose computer whose architecture is designed to best solve a specific problem. Another system--involved, for example, with atmospheric modeling, hydrodynamics design, or electronic device modeling and design--may opt for a general-purpose machine as the most reasonable and cost-effective solution. In either case,

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* Concept and estimates by F. Bedard, National Security Agency.

Table 3. Comparison of Silicon and LTS Estimated Power Requirements for IR Focal Plane Array*

	Computational Load**	Silicon Technology Power Requirement, watts	LTS Josephson Junction Technology Power Requirement, watts
Analog Signal Processing	800 MSPS†	1,500	0.05
Time-Dependent Processing	3×10^9 OPS†	7,500	3.4
Object-Dependent Processing	1.1 GFLOPS†	6,700	1.4
Mission-Dependent Processing	1.0 GFLOPS†	7,700	1.2
Subtotal		23,400 (at room temperature)	6.1 (cooled to 4.2 K)
Refrigeration		–	4,600
Total		23,400	4,606

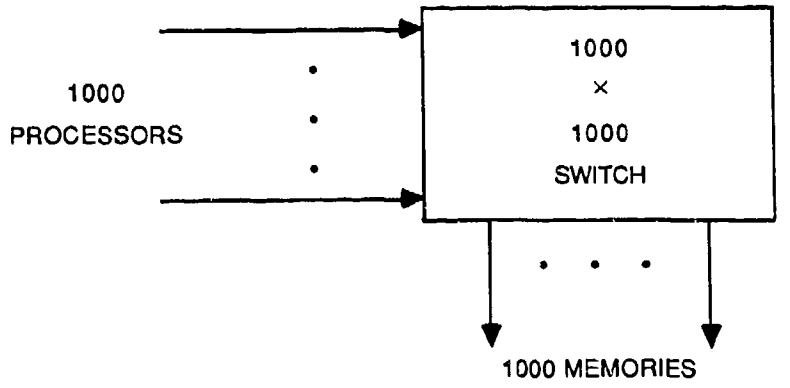
* Source: Ref. 10.

** Values from presentation by J. Grantham, Nichols Research Corporation, Huntsville, at SDIO/IST Superconductor Workshop, October 1989.

† MSPS = megasamples per second; OPS = operations per second; GFLOPS = giga floating operations per second.

modern computational needs are no longer met by conventional architectures that are centered on a small number of processors clocked at about a 4 nsec rate. The expectations are that future systems will require a large number of processors (for example, 1000) working in parallel and jointly accessing a shared memory bank (with, for example, 1000 memories) in order to achieve the required computational rate (Fig. 1). Such a system translates the severe stress imposed on the hardware by the very fast clock rates into a greatly reduced stress on the interconnection switch that joins the processors to the memories.

The "crossbar" switch, with its great versatility, is the candidate of choice for the interconnection. It provides for equal access of any processor to any memory line. This free and independent connection of P processors to M memories has $P \times M$ connection points, which quickly increase in number as the size of the system grows. As the number increases, so do the power dissipation problems and speed limitations that burden the



Size: 6 inch cube (approximately)
Power Dissipation: ~1 watt at 4 K

Figure 1. The 1000 × 1000 Crossbar Switch.

system. There is also the very stressing problem of operating in an "environment of contention" where a number of processors may request the same memory port at the same time. Dealing with that contention requires arbitration, which in turn requires additional hardware, either to reduce access time or to introduce elaborate preadjudication. Semiconductor technology would appear to face very difficult, if not insurmountable, obstacles in this situation. On the other hand, Josephson device technology with its aforementioned low power and high speed, coupled with superconducting transmission lines with their "zero" dispersion, would appear to provide a natural solution to the problem.

It should be possible to construct the 1000 × 1000 crossbar switch in superconductive technology to operate with about 1 watt power dissipation at 4 K. The switch would have the following performance features:

- Data Rate: ~2 Gb/sec per channel (i.e., ~2×10^{12} b/sec for a 1024 × 1024 switch)
- Access Time: ~10 nsec from input request to "acknowledge"/"reject" to return to processor
- Latency: ~10 nsec from input at switch to output at the memory port
- Arbitration: ~4 nsec to detect and "arbitrate" among all contenders
- Modularity: Easily expandable from 32 × 32 to ~1024 × 1024.

The crossbar switch requires input and output support electronics to interface with the processors and memories. These electronic supports could be at room temperature; their power consumption is not included in the above calculations.

In undertaking this demonstration system, one can begin with a 128 × 128 switch (Fig. 2) that is constructed of 32 × 32 modules. It would fit onto a 4-inch substrate, dissipate about 20 mW, and run at about 256 Gb/sec. The left processor glue (PG) chip allows 64 processors to access 64 memories via the top memory glue (MG) chip and another 64 memories via the bottom MG chip. Similarly, the remaining 64 processors enter from the right to access the same 128 memories.

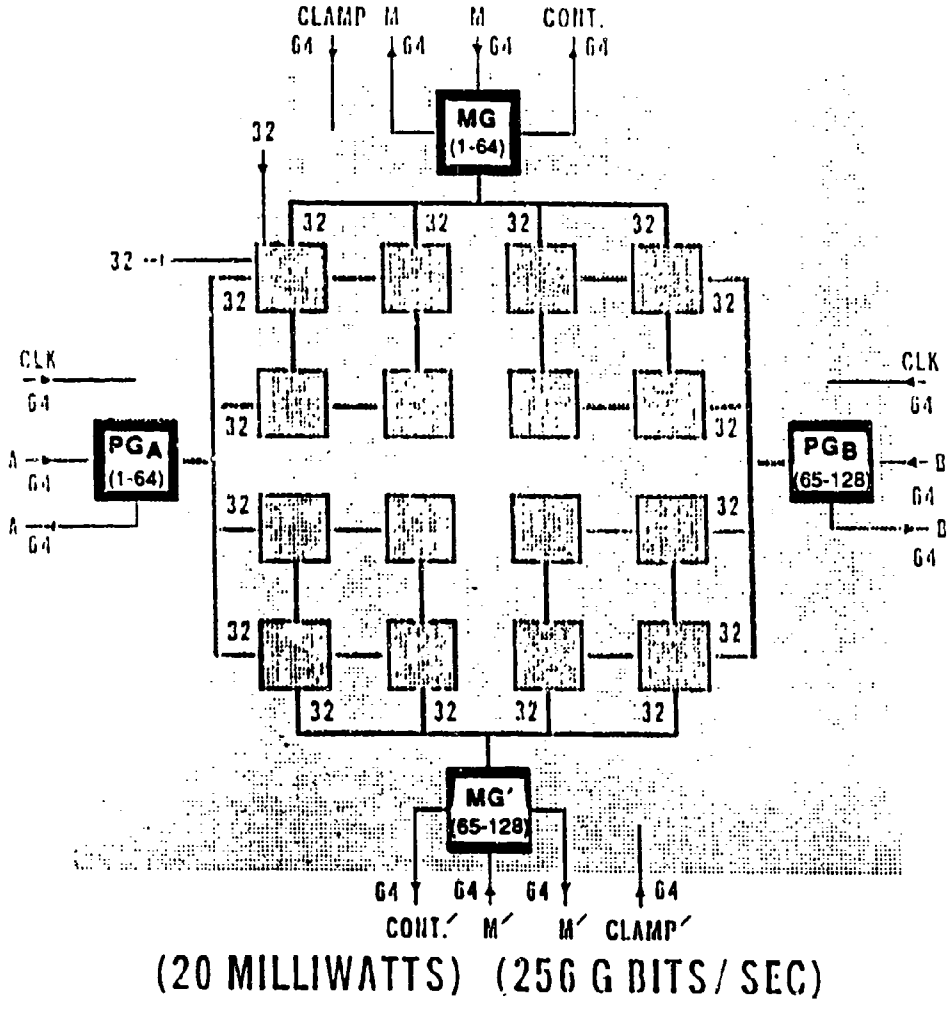


Figure 2. A 128 × 128 Crossbar Based on 32 × 32 Modules.

IV. SEFF AND DVs

The proposed Superconducting Electronics Fabrication Facility (SEFF) referred to in Chapters I and II is described in Ref. 1. Its essential features are briefly reviewed here. The facility would be established over a 5-year period in parallel with the development of an independent program that would target a series of demonstration vehicles (DVs) to be built by SEFF. The SEFF and DV programs would be mutually supportive. Initially a niobium line would be established at SEFF, and in the second or third year a niobium nitride line would be introduced. The inclusion of a high-temperature superconductor line would occur when the state of development of that technology permitted it. Over the 5-year period, design rules would be established and published. Gate densities would be taken from >100 to >5000 gates/chip. DVs would be selected in ascending order of complexity and fabricated. The DVs must be such that their successful fabrication will clearly show not only that superconducting electronics is a viable technology but also that both the right tools and the right people are in place to apply that technology to military systems. The two programs, for SEFF and the DVs, would be funded over the 5-year period at a total level of about $100 million.

V. CONCLUSIONS AND RECOMMENDATIONS

The salient features of current semiconductor technology and those of the evolving superconducting electronics technology are compared and discussed in this report. Semiconductor technology is nearing basic limits in dimensions, and therefore in component density. These limitations put further bounds on component speed and power dissipation. The three demonstration vehicles (DVs) cited in Chapter III of this paper illustrate the inadequacy of semiconductor electronics to handle the anticipated heavy computational requirements of future defense systems. The only visible technology that is a viable candidate to step in and supply the needs of future systems for circuits with greater speeds and much smaller power dissipations is superconducting electronics technology. The United States is far behind Japan in the evolution of this technology. It has no facility for fabricating circuits of the required complexity. Japan has at least four such facilities. The DoD could well find itself crippled by a dependency on offshore sources for circuits and devices for its future systems. To fend off that dependency and to develop a national resource in both circuits and skilled people, it is strongly recommended that the DoD establish SEFF and that a parallel program for making a preselected set of DVs of increasing complexity be initiated.

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